ABSTRACT

An integrated circuit memory including at least two banks each provided with an array of storage elements having at least one redundancy column and each associated with specific sense amplifiers, a row of input/output buffer circuits common to the memory banks, and for each memory bank, a circuit for assigning the redundancy column to an input/output line connected to one of said buffers. The assigning can be performed, for a line of current rank, towards the columns of preceding rank and towards the columns of following rank.